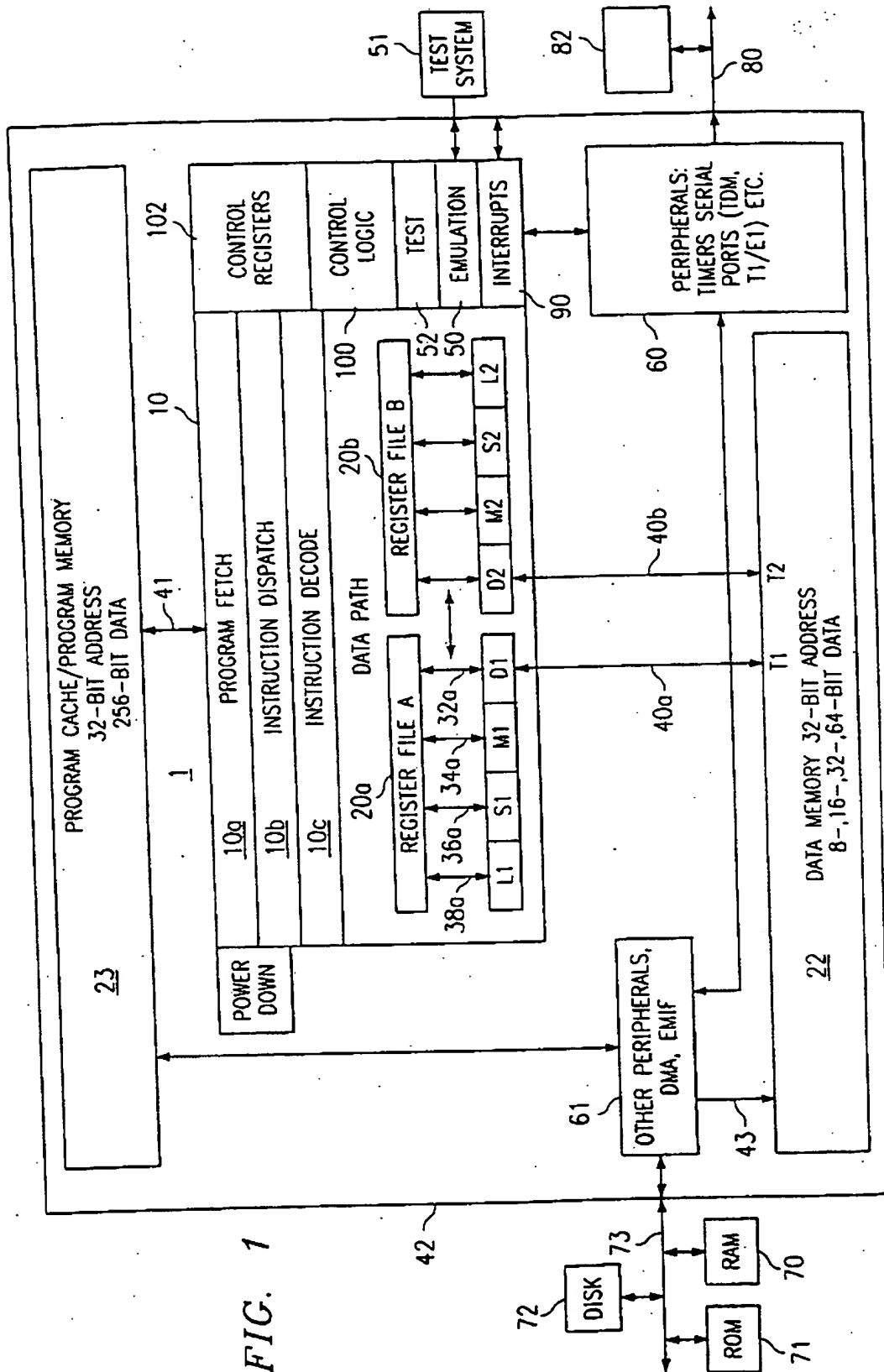


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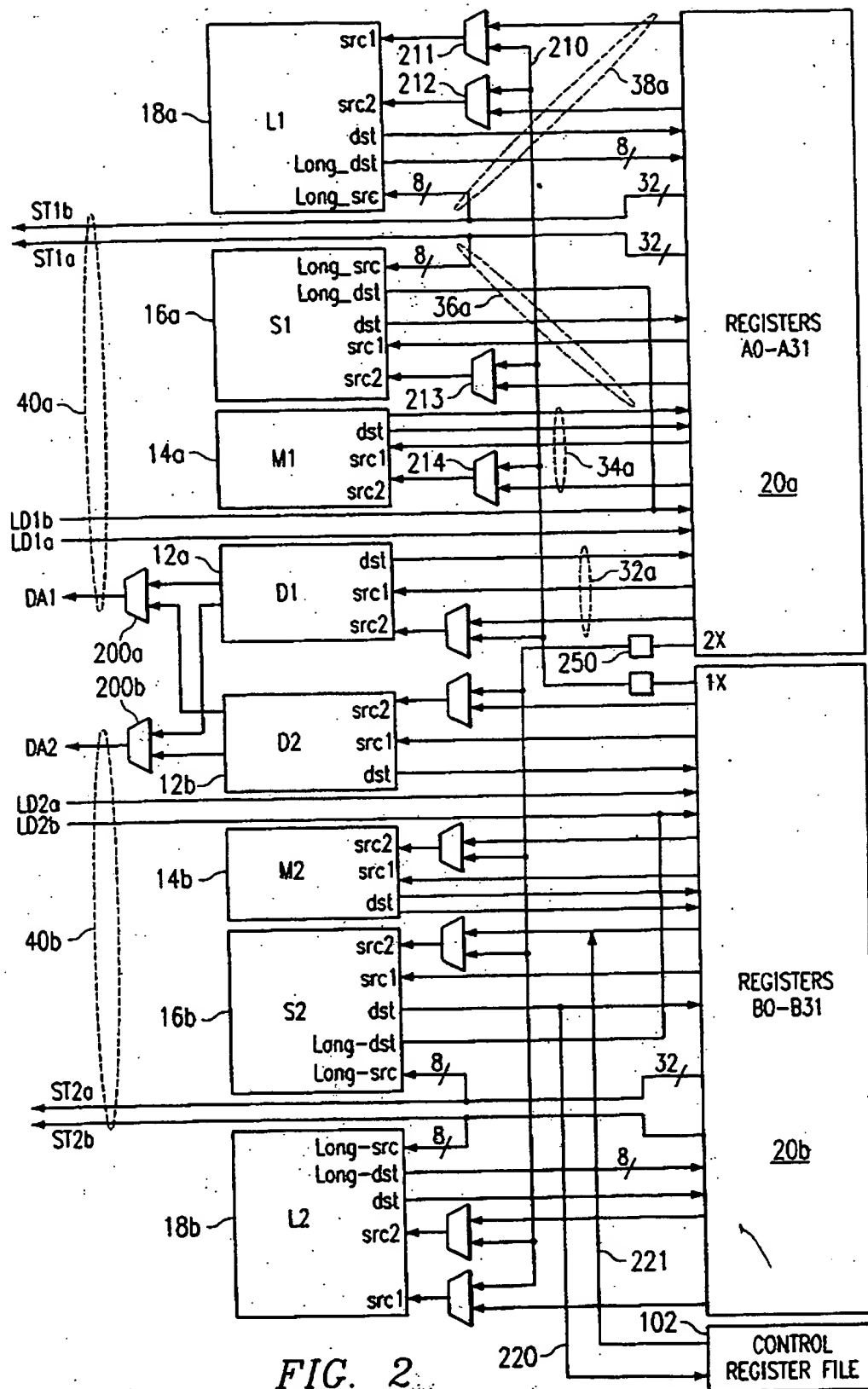


FIG. 2

OPERATIONS ON THE .L UNIT

31	29	28	27	23	22	18	17	13	12	11	5	4	3	2	1	0
CREG	Z	DST	SCR2	SRC1/CST	X	OP										
3	5	5	5	5	5	7										

FIG. 3A

OPERATIONS ON THE .M UNIT

31	29	28	27	23	22	18	17	13	12	11	7	6	5	4	3	2	1	0
CREG	Z	DST	SCR2	SRC1/CST	X	OP												
3	5	5	5	5	5	5												

FIG. 3B

OPERATIONS ON THE .D UNIT

OPERATIONS ON THE .D UNIT																	
31	29	28	27	23	22	18	17	13	12	7	6	5	4	3	2	1	0
CREG	Z	DST	SCR2	SRC1/CST	OP												
3	5	5	5	5	6												

FIG. 3C

LOAD/STORE WITH 15-BIT OFFSET (ON THE .D UNIT)

31	29	28	27	23	22	8	7	6	4	3	2	1	0
CREG	Z	DST/SRC	UCST15	Y	LD/ST	1	1	S	P				
3	5	15	3										

FIG. 3D

LOAD/STORE 'BASER' + 'OFFSETR/CST' ON THE .D UNIT

31	29	28	27	23	22	18	17	13	12	9	8	7	6	4	3	2	1	0
CREG	Z	DST/SRC	BASE R	OFFSET R/UCST15	MODE	R	Y	LD/ST	0	1	S	P						
3	5	5	5	5	4													

FIG. 3E

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OPERATIONS ON THE .S UNIT

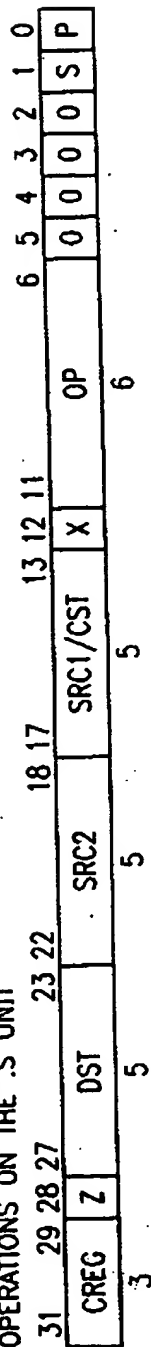


FIG. 3F

ADDK ON THE .S UNIT

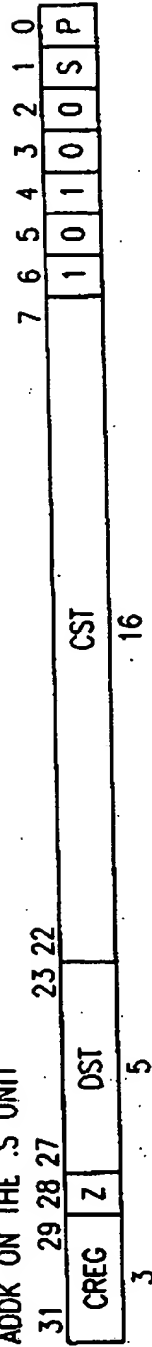


FIG. 3G

BITFIELD OPERATIONS (IMMEDIATE FORMS) ON THE .S UNIT

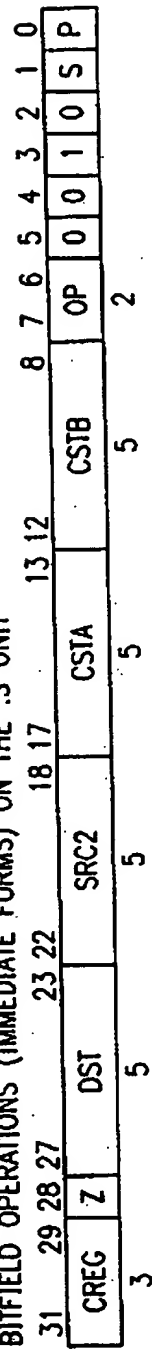


FIG. 3H

MVK AND MVKH ON THE .S UNIT

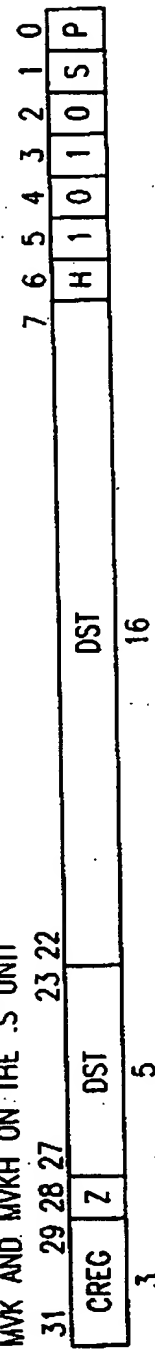


FIG. 3I

BCOND DISP ON THE .S UNIT

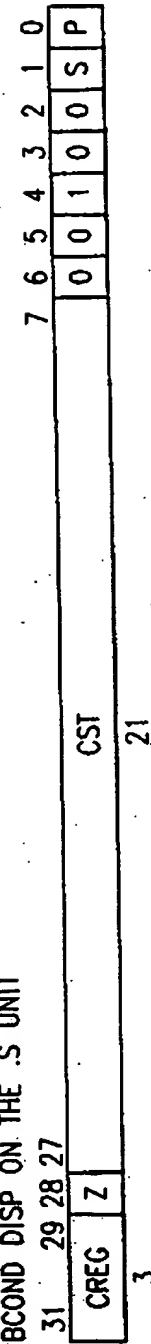


FIG. 3J

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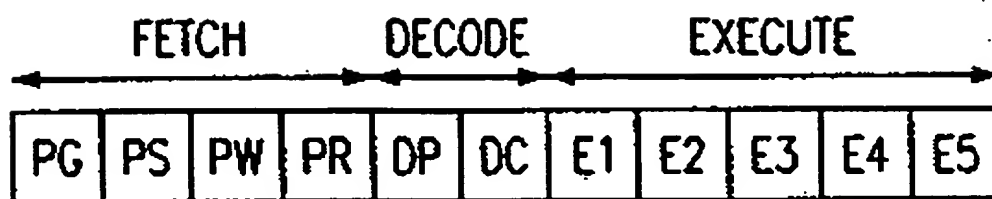


FIG. 4

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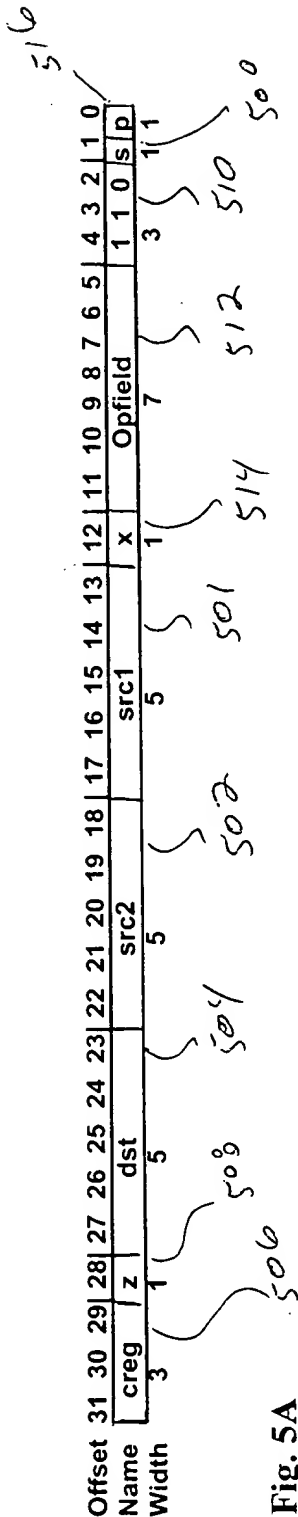


Fig. 5A

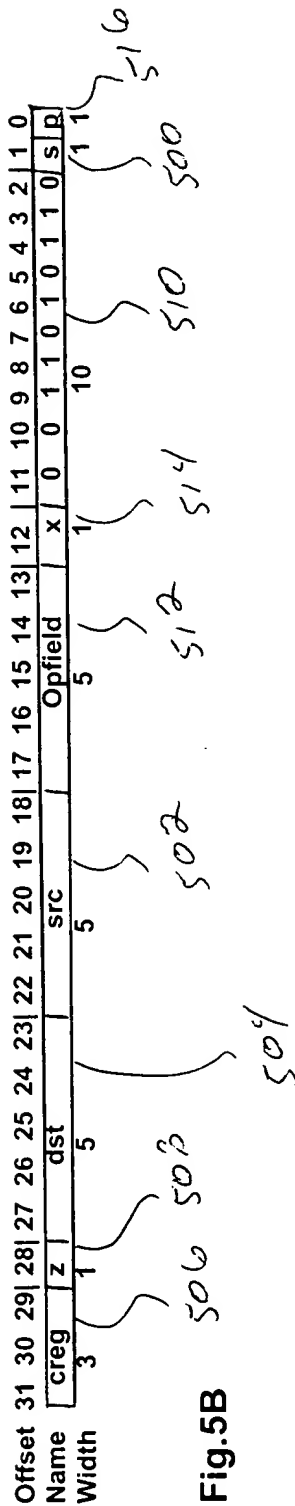


Fig. 5B

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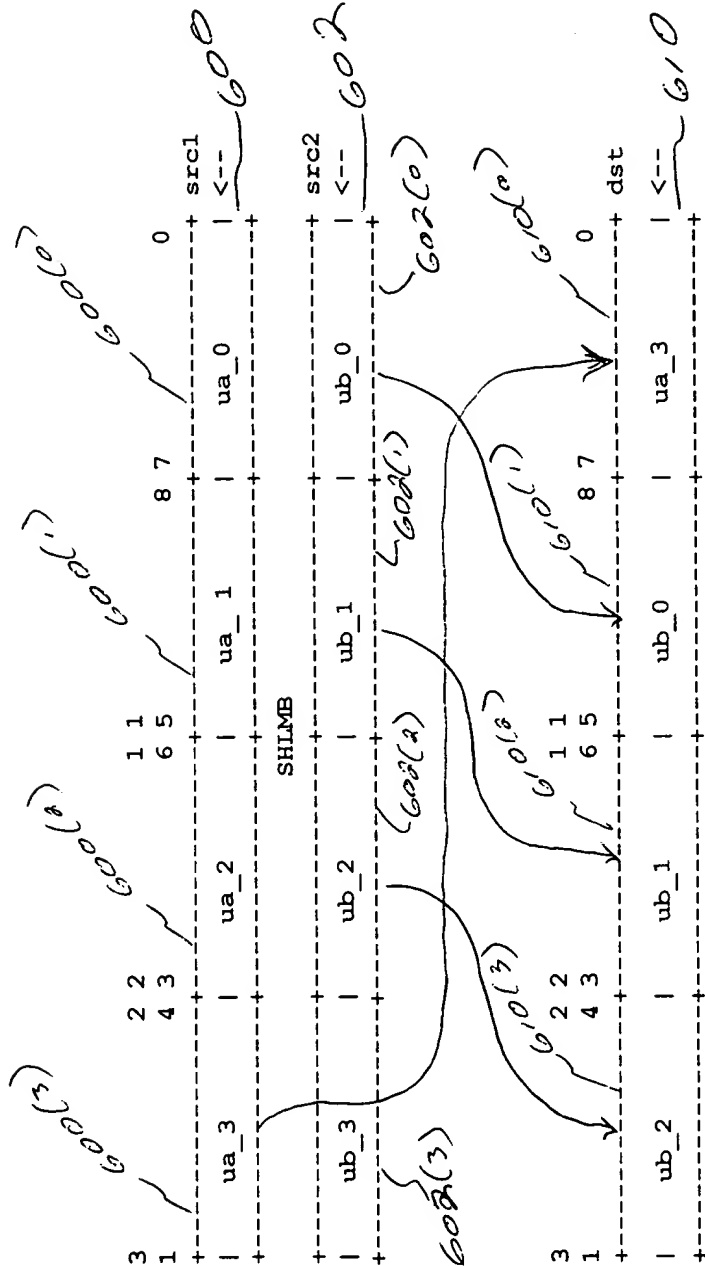


Fig. 6A

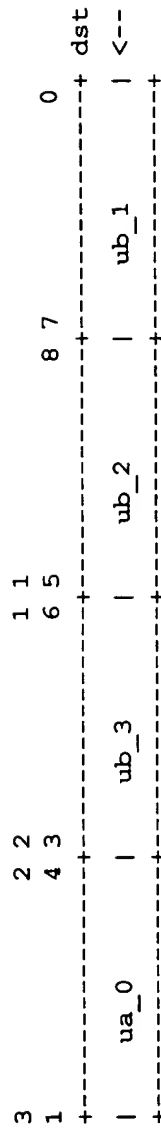


Fig. 6B

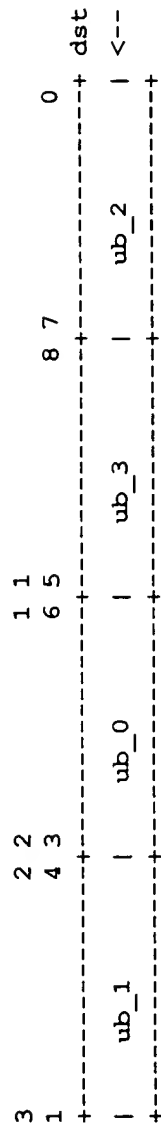


Fig. 6C

**00000000000000000000**

**Fig. 6D**

[illegible]

**Fig. 6E**

[illegible]

**Fig. 6F**

[illegible]

**Fig. 6G**

[illegible]

**Fig. 6H**

[illegible]

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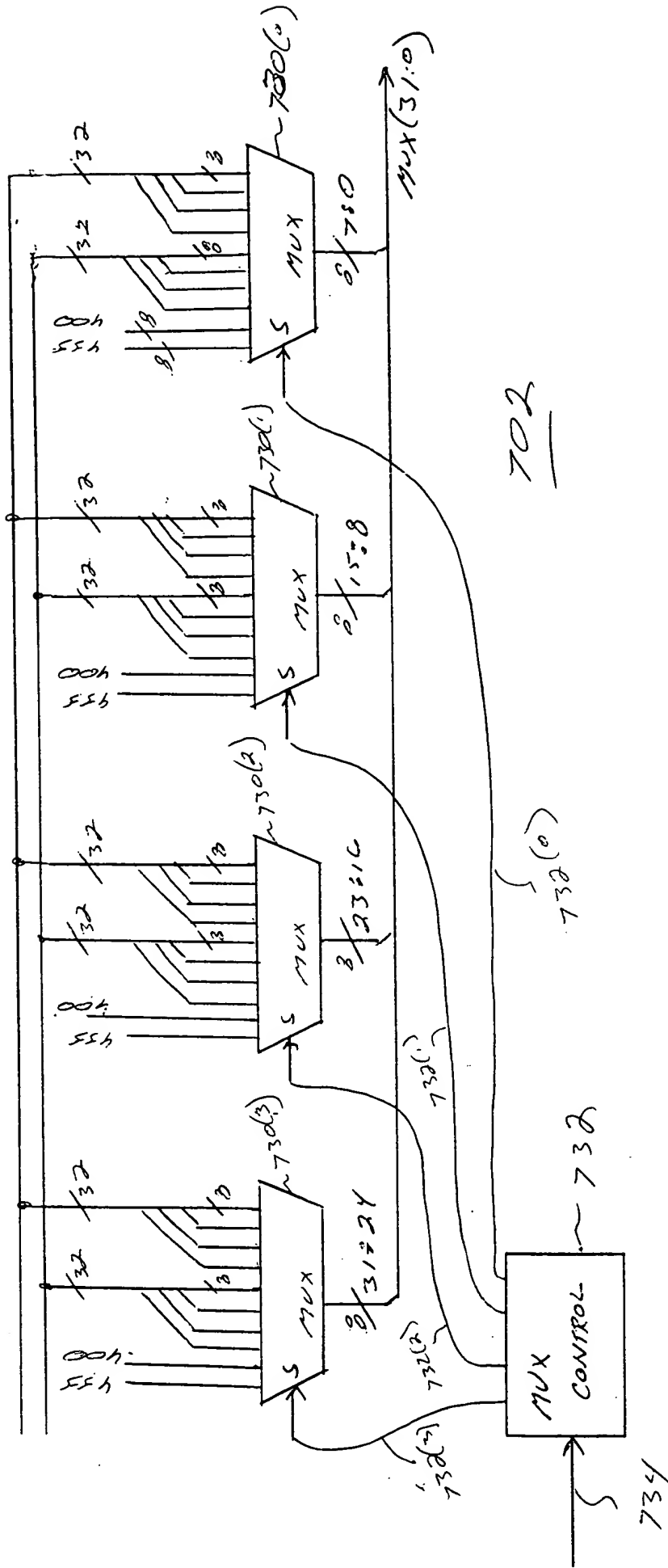


Fig 7B

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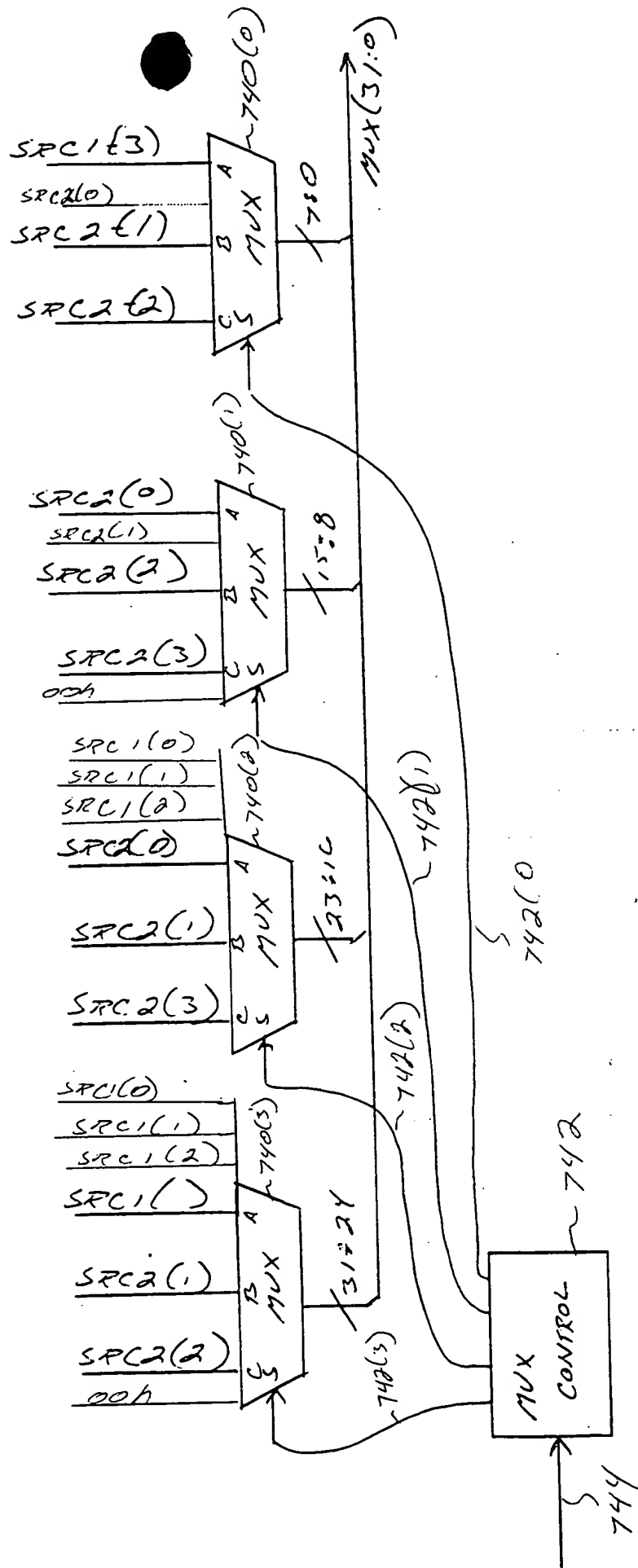


Fig. 7C

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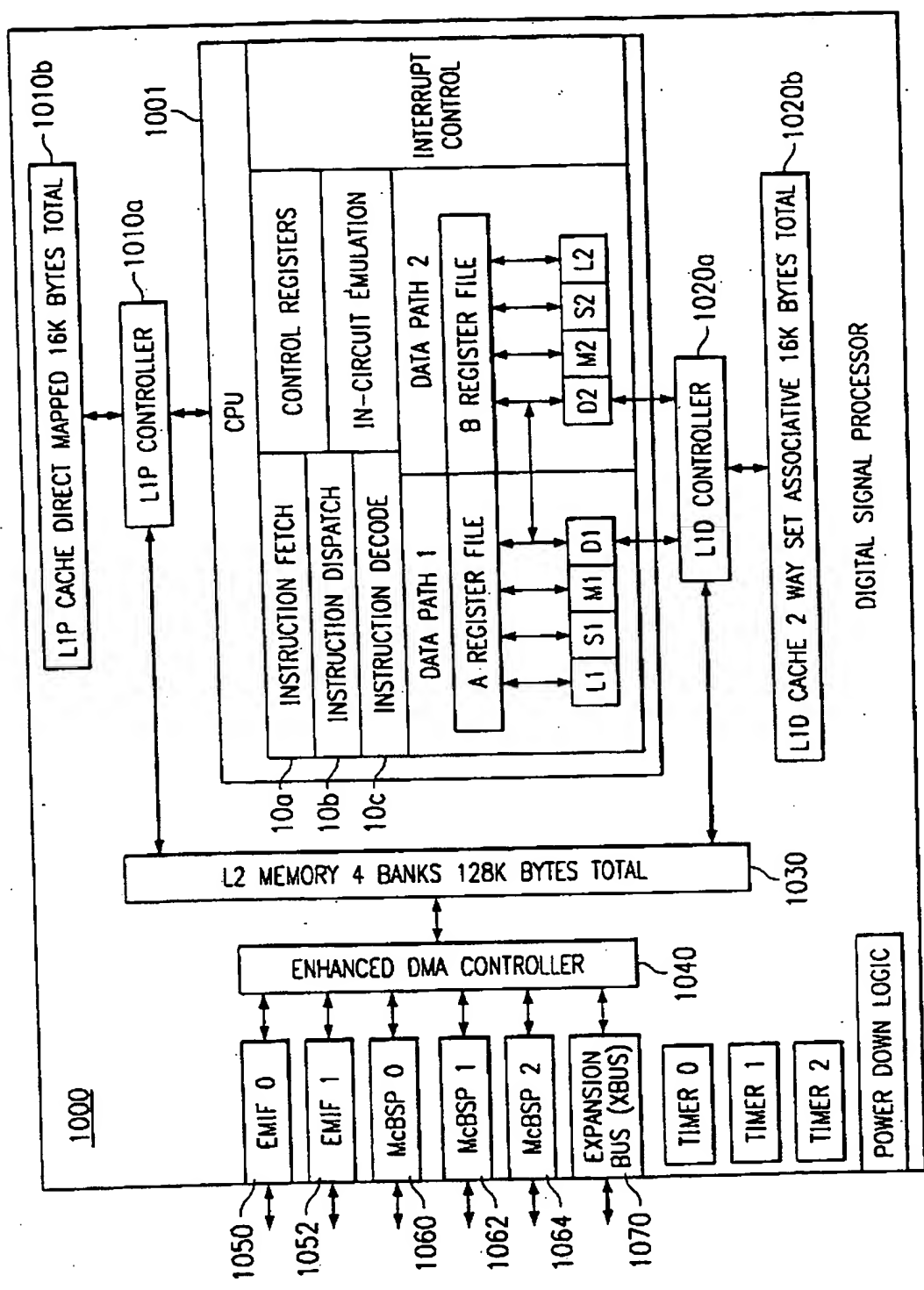


FIG. 3

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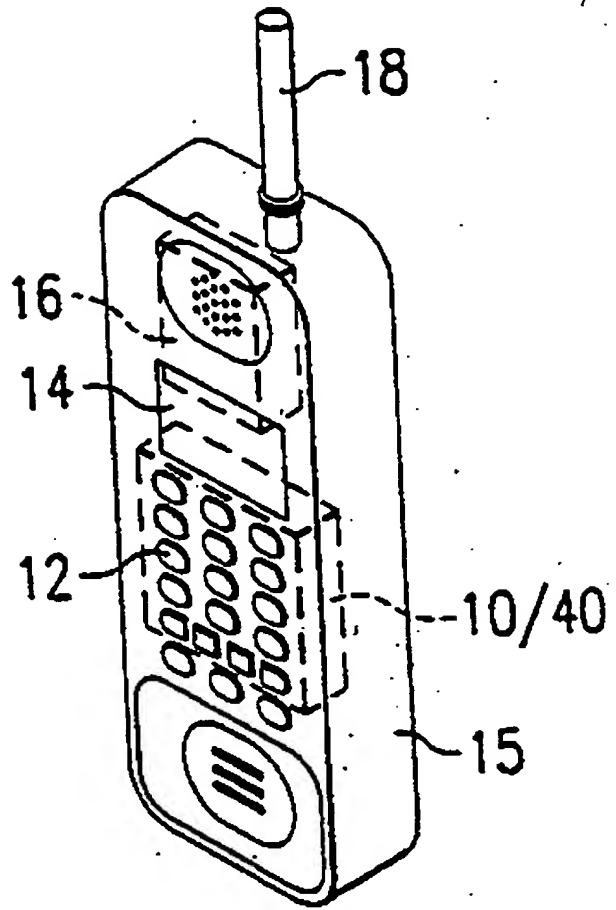


Fig 9

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